PD - 94520

International
IOR Rectifier

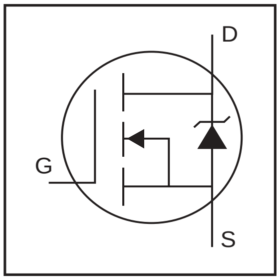
AUTOMOTIVE MOSFET

IRF1302S
IRF1302L

HEXFET® Power MOSFET

Benefits

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax



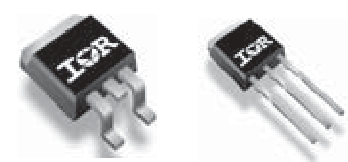
V_{DSS} = 20V

$R_{DS(on)}$ = 4.0mΩ

I_D = 174A⑥

Description

Specifically designed for Automotive applications, this Stripe Planar design of HEXFET® Power MOSFET utilizes the lastest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



D^2Pak
IRF1302S

TO-262
IRF1302L

Absolute Maximum Ratings

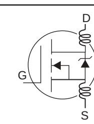
	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	174⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	120⑥	
I_{DM}	Pulsed Drain Current ①	700	
P_D @T_C = 25°C	Power Dissipation	200	W
	Linear Derating Factor	1.4	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	350	mJ
I_{AR}	Avalanche Current①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy⑦		mJ
dv/dt	Peak Diode Recovery dv/dt ③	TBD	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

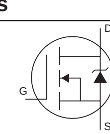
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.74	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)⑧	——	40	

07/16/02

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.021	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	3.3	4.0	mΩ	V_{GS} = 10V, I_D = 104A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = 10V, I_D = 250µA
g_{fs}	Forward Transconductance	59	——	——	S	V_{DS} = 15V, I_D = 104A
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	µA	V_{DS} = 20V, V_{GS} = 0V
		——	——	250		V_{DS} = 16V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-200		V_{GS} = -20V
Q_g	Total Gate Charge	——	79	120	nC	I_D = 104A
Q_{gs}	Gate-to-Source Charge	——	18	27		V_{DS} = 16V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	31	46		V_{GS} = 10V④
$t_{d(on)}$	Turn-On Delay Time	——	28	——	ns	V_{DD} = 11V
t_r	Rise Time	——	130	——		I_D = 104A
$t_{d(off)}$	Turn-Off Delay Time	——	47	——		R_G = 4.5Ω
t_f	Fall Time	——	16	——		V_{GS} = 10V ④
L_D	Internal Drain Inductance	——	4.5	——	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	——	7.5	——		
C_{iss}	Input Capacitance	——	3600	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	2370	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	520	——		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	——	5710	——		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	——	2370	——		V_{GS} = 0V, V_{DS} = 16V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance ⑤	——	3540	——		V_{GS} = 0V, V_{DS} = 0V to 16V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	174⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	700		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 104A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	66	100	ns	T_J = 25°C, I_F = 104A
Q_{rr}	Reverse RecoveryCharge	——	130	200	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

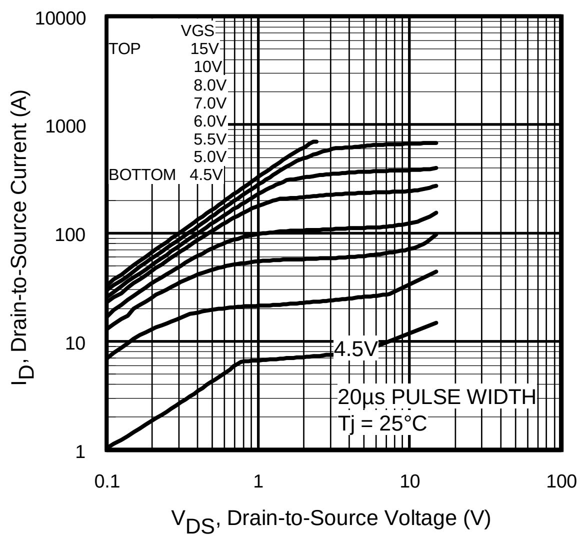


Fig 1. Typical Output Characteristics

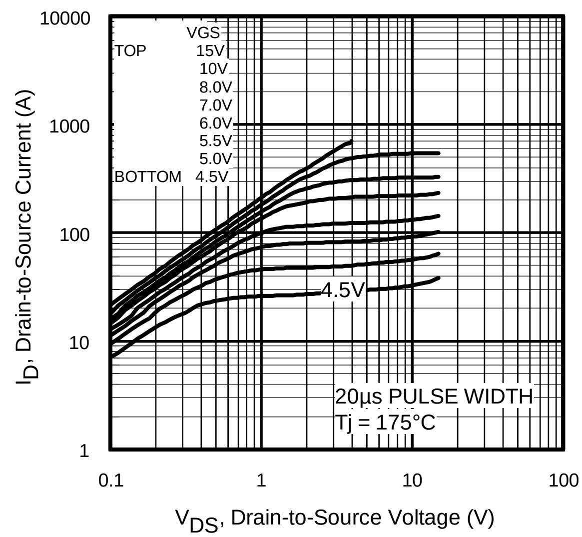


Fig 2. Typical Output Characteristics

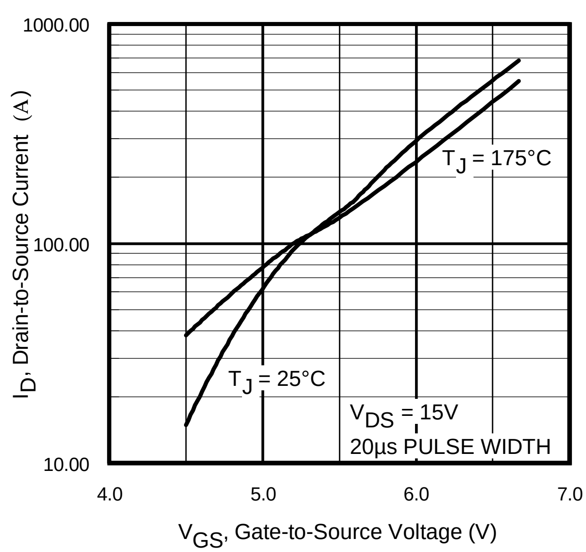


Fig 3. Typical Transfer Characteristics

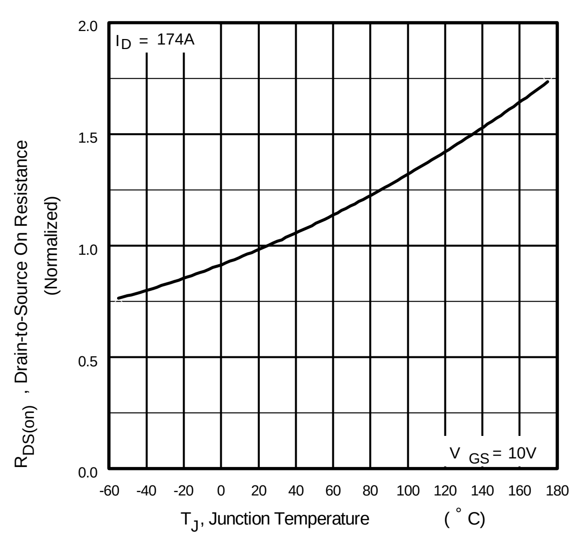


Fig 4. Normalized On-Resistance
Vs. Temperature

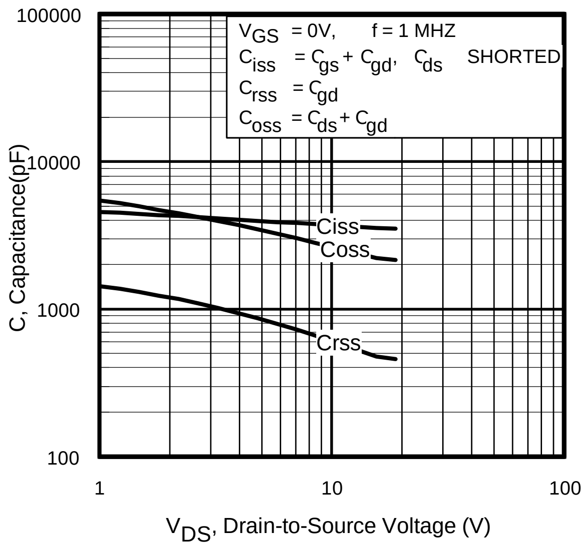


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

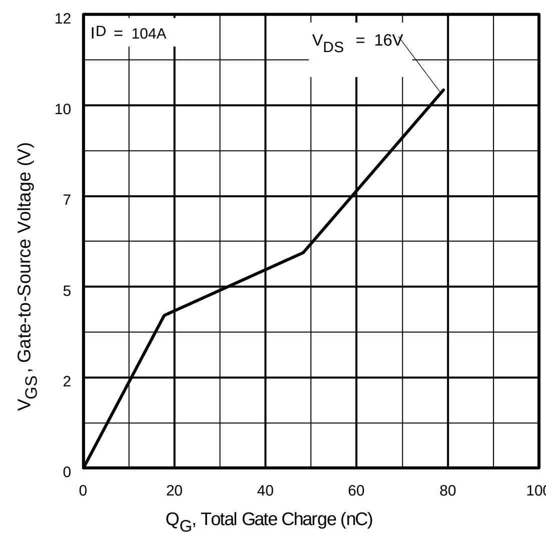


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

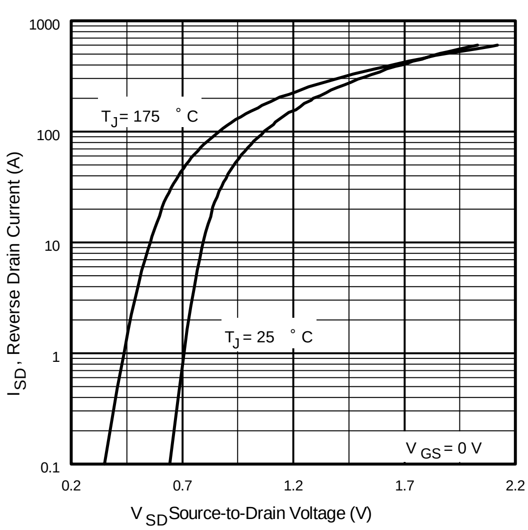


Fig 7. Typical Source-Drain Diode Forward Voltage

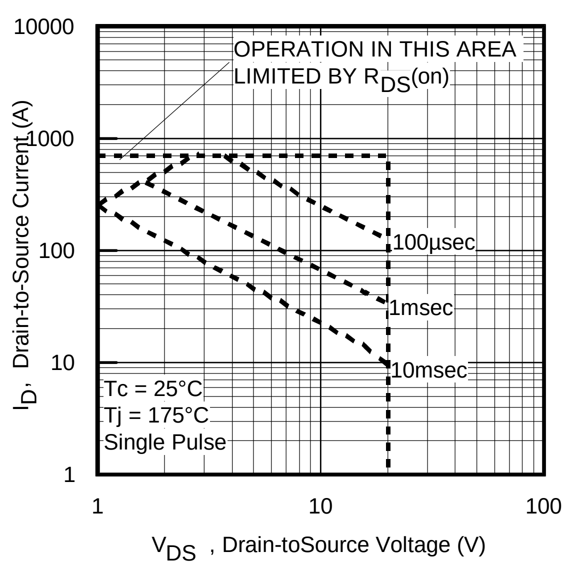


Fig 8. Maximum Safe Operating Area

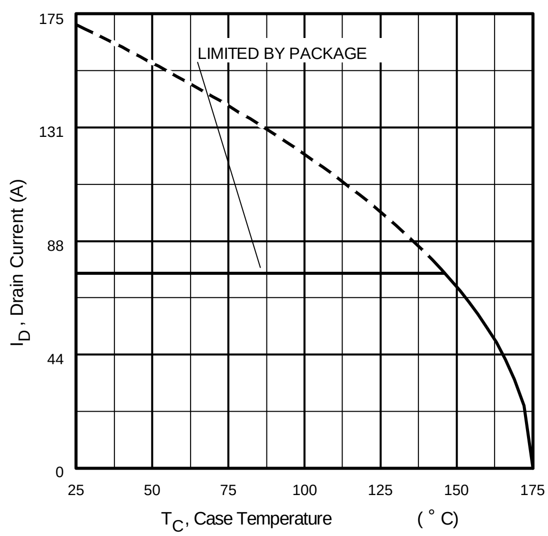


Fig 9. Maximum Drain Current Vs. Case Temperature

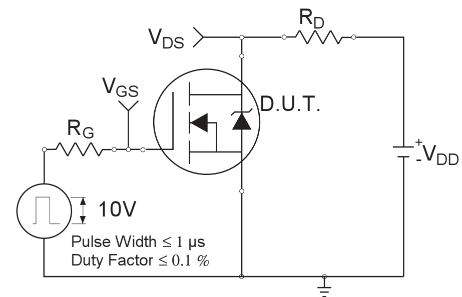


Fig 10a. Switching Time Test Circuit

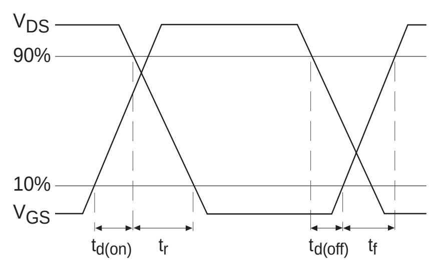


Fig 10b. Switching Time Waveforms

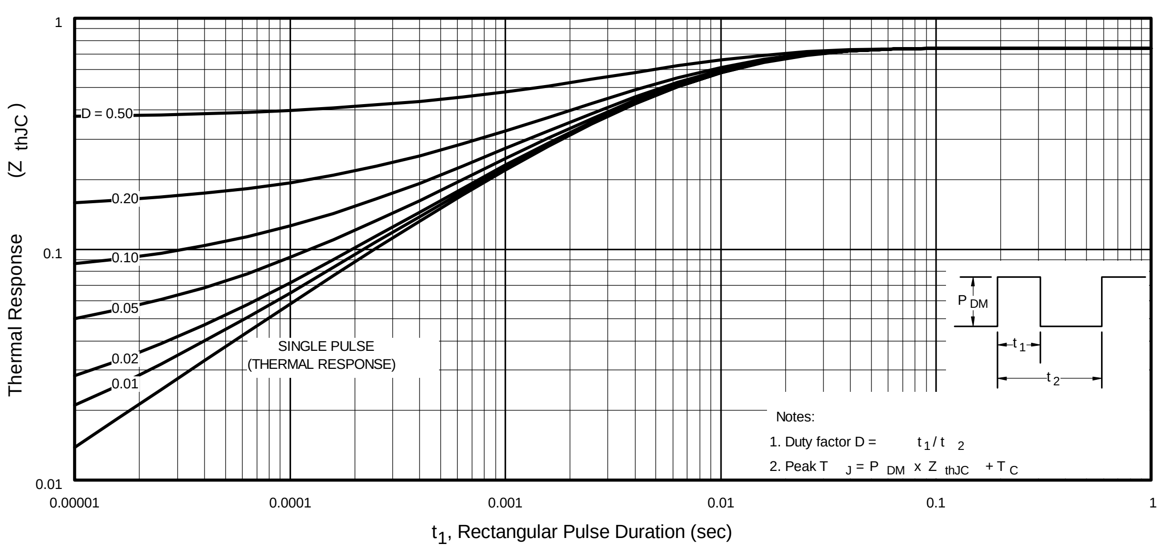


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

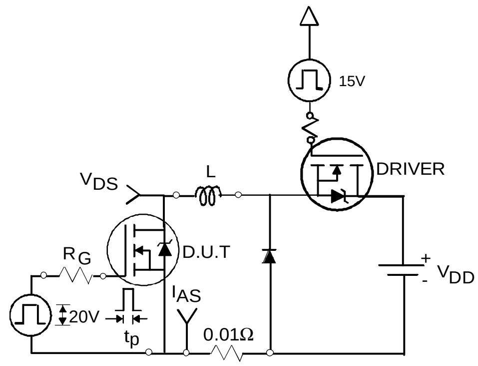


Fig 12a. Unclamped Inductive Test Circuit

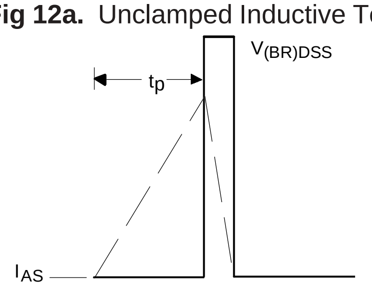


Fig 12b. Unclamped Inductive Waveforms

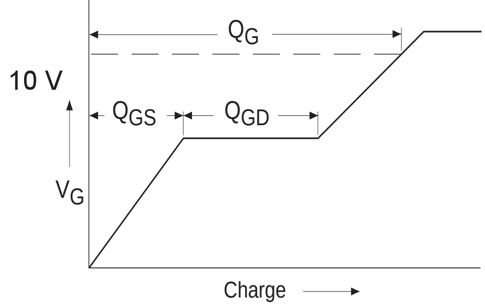


Fig 13a. Basic Gate Charge Waveform

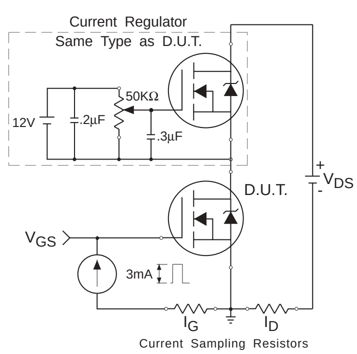


Fig 13b. Gate Charge Test Circuit

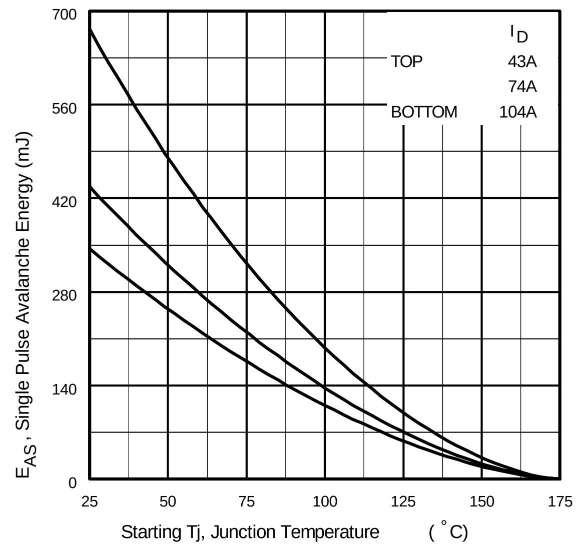


Fig 12c. Maximum Avalanche Energy
Vs. Drain Current

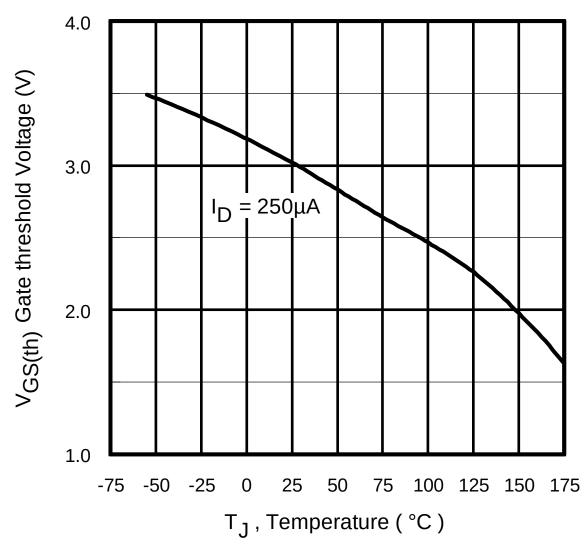


Fig 14. Threshold Voltage Vs. Temperature

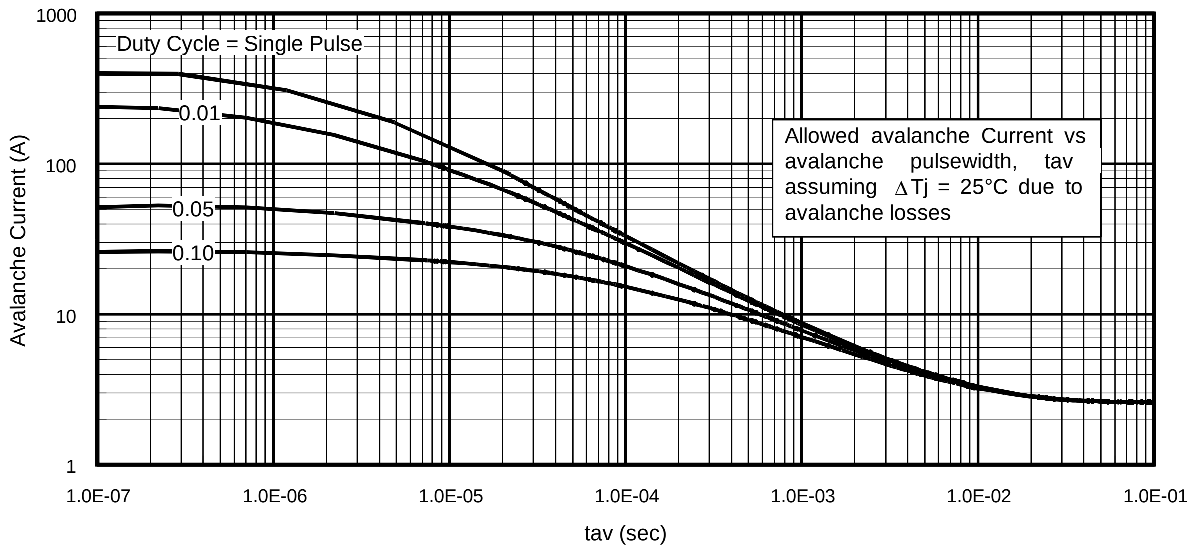


Fig 15. Typical Avalanche Current Vs.Pulsewidth

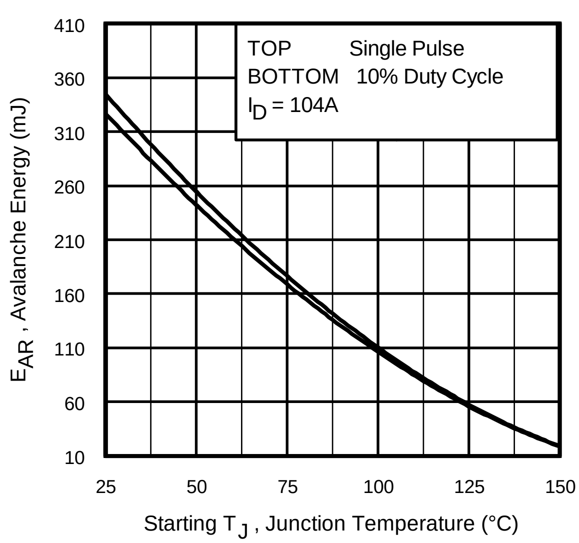


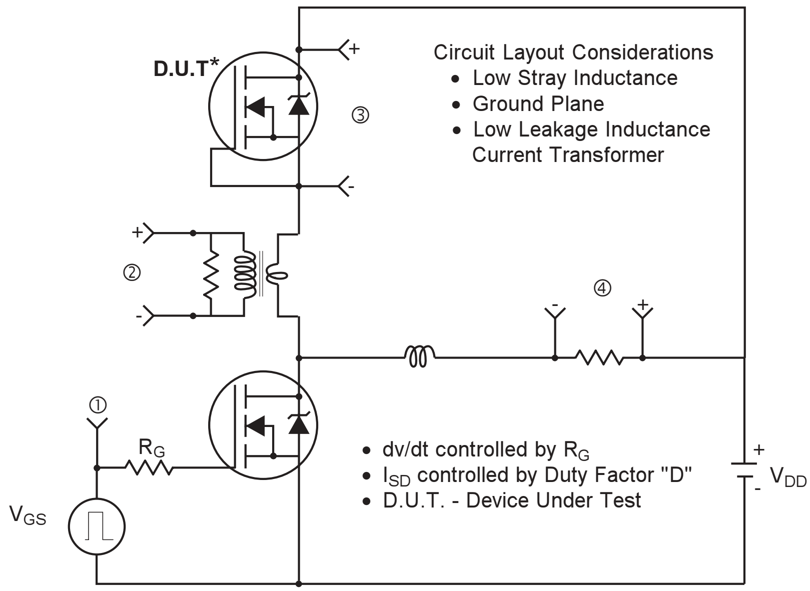
Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

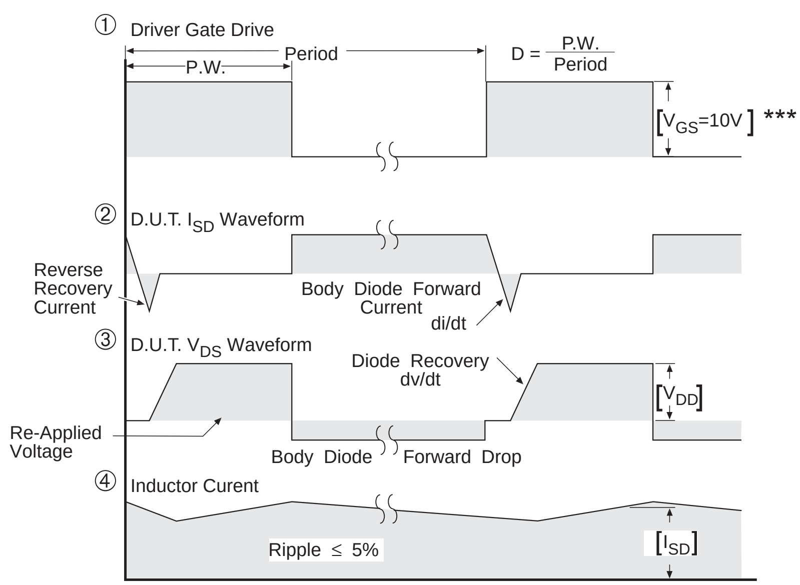
1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

Peak Diode Recovery dv/dt Test Circuit



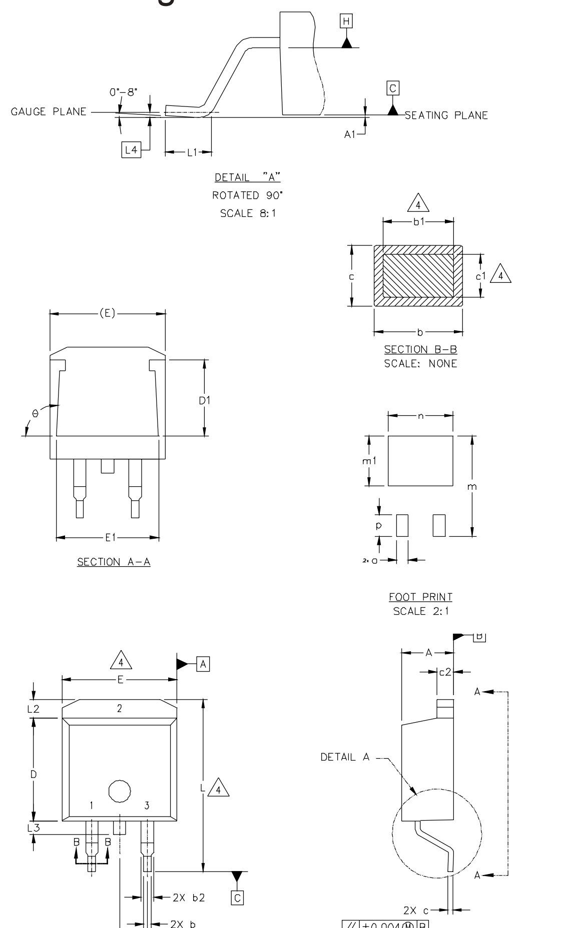
* Reverse Polarity of D.U.T for P-Channel



*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 17. For N-channel HEXFET® power MOSFETs

D2Pak Package Outline

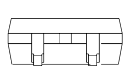


S Y M B O L	DIMENSIONS				N O T E S
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1		0.127		.005	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.38	0.74	.015	.029	
c1	0.43	0.63	.017	.025	4
c2	1.14	1.40	.045	.055	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	
L2		1.65		.065	
L3	1.27	1.78	.050	.070	
L4	0.25 BSC		.010 BSC		
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
θ	90°	93°	90°	93°	

LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK	DIODES
1.– GATE	1.– GATE	1.– ANODE *
2.– DRAIN	2.– COLLECTOR	2.– CATHODE
3.– SOURCE	3.– EMITTER	3.– ANODE

* PART DEPENDENT.

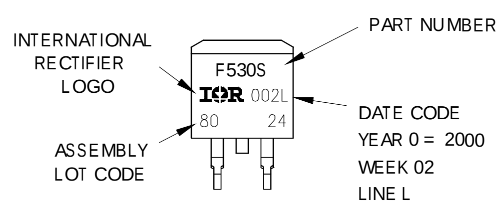


NOTES:

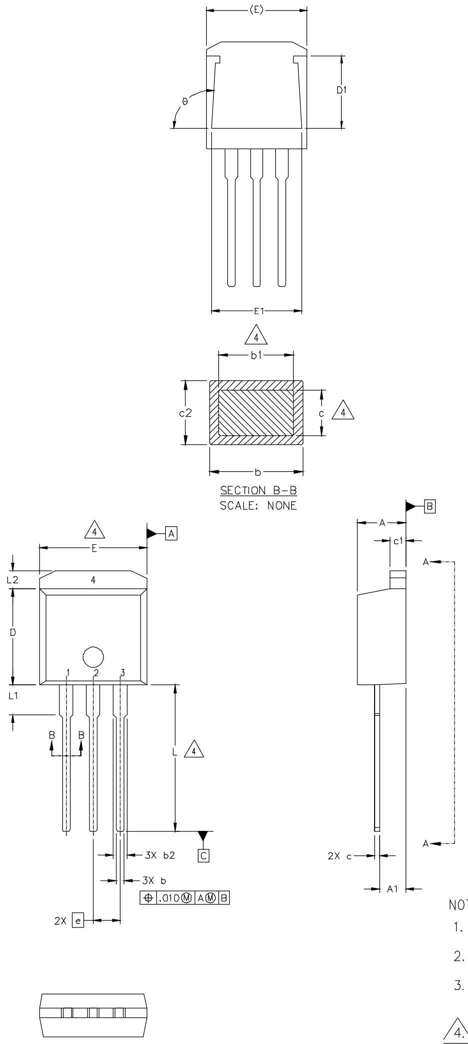
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

D2Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"



TO-262 Package Outline



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.38	0.63	.015	.025	4
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

LEAD ASSIGNMENTS

HEXFET

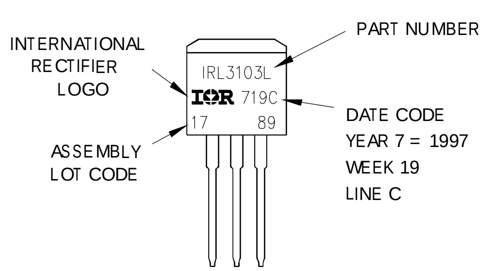
1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

NOTES:

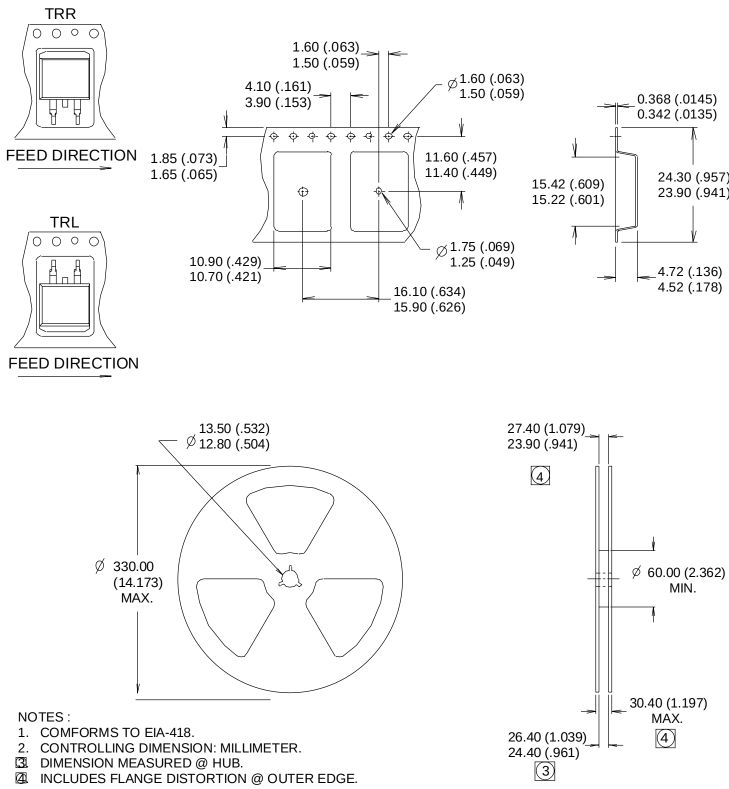
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



D^2Pak Tape & Reel Information



Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Starting $T_J = 25°C$, $L = 0.063mH$ $R_G = 25\Omega$, $I_{AS} = 104A$. (See Figure 12).

③ $I_{SD} \le 104A$, $di/dt \le 100A/\mu s$, $V_{DD} \le V_{(BR)DSS}$, $T_J \le 175°C$.

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

⑦ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

⑧ This is applied to D^2Pak, when mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

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